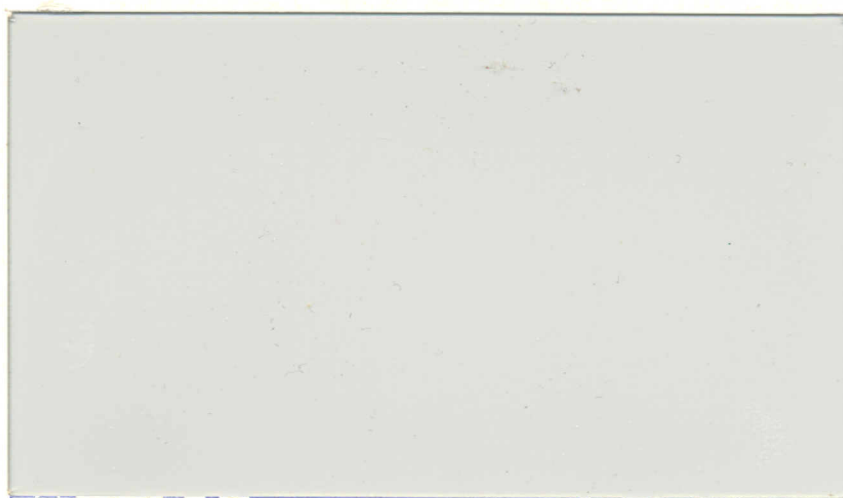




QBX-PCC

PARALLEL I/O,
CLOCK AND JULIAN CALENDAR

USER MANUAL

QBX-PCC

Product:- QBX-PCC
Product Number:- 1001
Manual Number:- 1001-01

Chapter	Rev	Note
All	1.0	1
all	1.1	2

Notes:-

- 1.Original Document
- 2.Spelling corrections, R&D interchange with Quantum, use of LP339, change of R&D phone number

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c/o R & D Electronics (Pty) Ltd.,
P.O. Box 61903,
Marshalltown 2107,
Johannesburg, South Africa.
Telex: 8-3046 SA Phone: 8347212

Rev:1.1

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CHAPTER 1 GENERAL

Introduction

The QBX-PCC board is one of the growing range of iSBX bus compatible boards manufactured by R & D Electronics. These boards are designed to increase the number of functions in a Multibus system without having to resort to the addition of a full sized Multibus board to achieve that function. This document along with the Intel 8255A data sheet provides all the information required to use the QBX-PCC.

Description

The QBX-PCC provides the Multibus user with the often needed function of a clock and Julian clock calendar. Once programmed the information is maintained by means of a rechargeable NiCd battery. The timekeeping function is performed by the NEC 1990AC chip. The interface to this device is via an 8255A-5. Since only some of the 24 I/O lines of the 8255 are used the remainder are brought out to an edge connector via buffers for the user.

The timekeeping functions performed are: seconds, minutes, hours, day of week and months. In the section on programming information the possibility of leap year adjustment and year storage is discussed. The timekeeping device is also capable of providing periodic interrupts.

Equipment Supplied

The QBX-PCC is shipped in a padded package. Included in this package are a plastic spacer and two plastic screws to mount the QBX board onto the host computer.

Shipping Configuration

The QBX-PCC is shipped tested but the crystal on the QBX-PCC has not been trimmed. Optional ICs 4 and 5 are not supplied. Whilst the on board battery is supplied it is not connected.

Specifications

Access Time:

Read time 250 nS
Write time 300 nS

Addressing Range:

The QBX-PCC is compatible with any board that supports the Intel iSBX bus. The addressing range of the QBX-PCC is derived from this host board.

Interface:

System Bus compatible with the SBX bus specifications. See Intel publication 142686-001

I/O lines

Port A 8 lines brought out to 26 way connector via 74LS245 (optional)
Port C 5 lines brought out to 26 way connector via 7407 /7404 (optional)
direction driver for 74LS245
external battery connection

Interface Connectors:

13/26 way, 0.1 inch spacing, compatible with Robinson Nugent IDE-26 or similar.

Power Requirements:

5V +/-5% @151mA -depends on charging rate of battery, and without ICs 4 and 5 installed.

Battery requirement: battery voltage between 1.8V and 3.6V. At 3.6V worst case current drain is 2.1mA. The on board battery is guaranteed to maintain data for 3 days when fully charged.

Can be considerably improved by replacing LM339 with LP339

Crystal:

Nominal Frequency: 32768 Hz +/- 15 ppm
Vibration Resistance: +/- 2ppm
Shock Resistance: +/-2 ppm
Ageing (per year): +/- 2ppm

Battery:

2.4V Nicd 150mAH nominal

Environment:

Operating temperature 0 to 55 degrees Celsius, humidity 5 - 90% non condensing.

Size:

Width: 721mm (2.84 in)
Length: 944mm (3.72 in)
Height: 20.6mm (0.81 in)
Weight:

CHAPTER 2 PRINCIPLE OF OPERATION

Introduction

This chapter describes the hardware operation of the QBX-PCC. It would be advisable for this and the next chapter to have a copy of the Intel 8255A data sheet with programming information.

QBX Bus Interface

Detailed description of the iSBX is contained in the Intel publication 142686-001. Users are referred to this document for a thorough description of this bus. The QBX-PCC utilises the following signals: MD0-MD7, AD0, AD1, IOWR/, IORD/, CS0/, MINTR0, MINTR1, MRESET and of course MPST/, ground and +5V.

Software Interface

All communications with the QBX-PCC is via the four registers of the 8255A. Access to them is controlled by CS0/ being active simultaneously with the read or write command. MA0 and MA1 control which register is being accessed.

NEC 1990

The NEC 1990 is a device that contains all the circuitry necessary to maintain the time and date up to and including the months of the year. The timekeeping operation is maintained accurately by a 32.768 KHz ceramic crystal. The power to this device must be between 1.8V and 3.6V for it to operate properly. The NiCd battery serves to clamp the supply voltage to this chip when the external power is on.

The method of communication with this device is via a 40 bit shift register contained on chip, and 3 command lines. Data to and from the shift register is clocked by the CK line and each instruction to perform a separate function is strobed by means of the STB line.

Data are shifted in or out of the 40 bit shift register on the low to high CK transition. The instruction is loaded by the low to high edge of the STB signal.

Figure 2.1 gives a block diagram of the 1990.

Port B is used to control the inputs to the device. Because the 1990 operates at a reduced voltage, current limiting resistors are placed in series with the inputs to prevent device failure. Port C bit 0 is used for the output from the shift register. This output is open drain and can be pulled up to 5 volts to allow direct interface to the 8255A. It can be seen from this that in programming the 8255A port B must be set to MODE 0, output and port C lower to input.

Table 2.1 provides a list of the different functions controlled by the different bits of port B and C

Port B	Function on 1990
B0	CK - clock data in or out
B1	Din - data in to shift register
B2	STB - strobe instruction
B3	C0 - 1 of 3 bit instruction
B4	C1 - "
B5	C2 - "
Port C	
C0	Dout - data out of shift register

Table 2.1
Functional allocation of Ports B and C

Interrupts

The 1990 clock chip is capable of generating periodic waveforms on both the data out and another pin entitled TP. In the handshake mode the 8255A generates an interrupt on PC3. Any of these may be jumpered to MINT0 or MINT1 to provide interrupts to the microprocessor. The interrupt outputs are indicated by I0 and I1 on the QBX-PCC board, whilst PC3 is indicated as C3 (ambiguously as there is a C3 capacitor on the board next to IC5). DO represents Dout. All 5 jumper pads are located in the region of the QBX connector, mainly near the 1990 (IC2).

Uncommitted I/O

Port A and Port C bits 3-7 are brought to an edge connector via optional buffers. These are not installed as each user will want a different configuration. Table 2.2 provides information on the devices that may be used, if required.

IC5	Attributes	IC4	Attributes
7404	I	74LS245	B
7406/16	I,OC	8T125	B,I
7407/17	OC		

I=Inverting, OC=Open Collector, B=Bi-directional

Table 2.2
Optional Devices for IC4 and IC5

Table 2.3 provides a summary of the port addresses of the 8255A.

Binary I/O Address	Function
VWZY0X11	Control
VWZY0X10	Port C
VWZY0X01	Port B
VWZY0X00	Port A

Table 2.3
Summary of Port Addresses

IC4 is permanently enabled (if installed). The direction of buffer data flow may be permanently set by jumpering pad E to pad A or B (ground and Vcc respectively). Alternatively if it is jumpered to pad E the direction may be altered externally. By altering the connections around pads F,G,H,J (see schematic) the logic sense may be changed, to allow data out on low or high and the reverse for data in.

Table 2.4 gives the pinout of the functions at the edge connector. Note that the pin numbers do not correspond to the pin numbers normally used on a ribbon cable connector.

Function	Edge connector	Description
BPA0	12	Buffered PA0
BPA1	14	Buffered PA1
BPA2	16	Buffered PA2
BPA3	18	Buffered PA3
BPA4	10	Buffered PA4
BPA5	20	Buffered PA5
BPA6	22	Buffered PA6
BPA7	24	Buffered PA7
BPC3	9	Buffered PC3
BPC4	11	Buffered PC4
BPC5	4	Buffered PC5
BPC6	6	Buffered PC6
BPC7	8	Buffered PC7
Pad D	26	for uninverted direction control of IC 4
Pad F	2	for inverted direction control of IC 4
ground	3,5,7	system ground
Vbatt	1	connection for external battery (disconnect on board battery)

Table 2.4
Pin Allocation on Edge Connector

Jumper Pad	Description
E-B	data from 8255 off the board, Data out
E-A	data onto board to 8255, Data in
E-D	external direction control
F-H	direction control to inverter input
F-J	direction control bypasses inverter
G	remember to drill out through hole to break connection to output of IC5/12

Table 2.5
Pad Configuration

Power Fail

When Vcc drops below 4.5V the output of the comparator IC3/2 goes low and inhibits any operation on the 1990. In a similar manner whenever a reset occurs any action on the 1990 is also prevented. This is to guarantee time integrity on power on and power off.

Battery Considerations

The battery is a 2.4V NiCd with a nominal capacity of 150mAH. Worst case current is 2.1mA yielding 72 hours. If this is to be extended add a battery of larger capacity via the edge connector and disconnect the on board battery. Beware that the voltage on pin 14 of the 1990 (IC2) does not exceed 3.6V. Resistors R1 and R2 (used for detection of power fail) may have to be adjusted to compensate for a change in voltage.

R3 may have to be removed if the off board battery is non rechargeable or is charged from a different source. R3 may also be altered for different charge rates.

The length of time that the clock will operate for on the battery can be extended considerably by replacing the LM339 comparator with the National Semiconductor LP339.

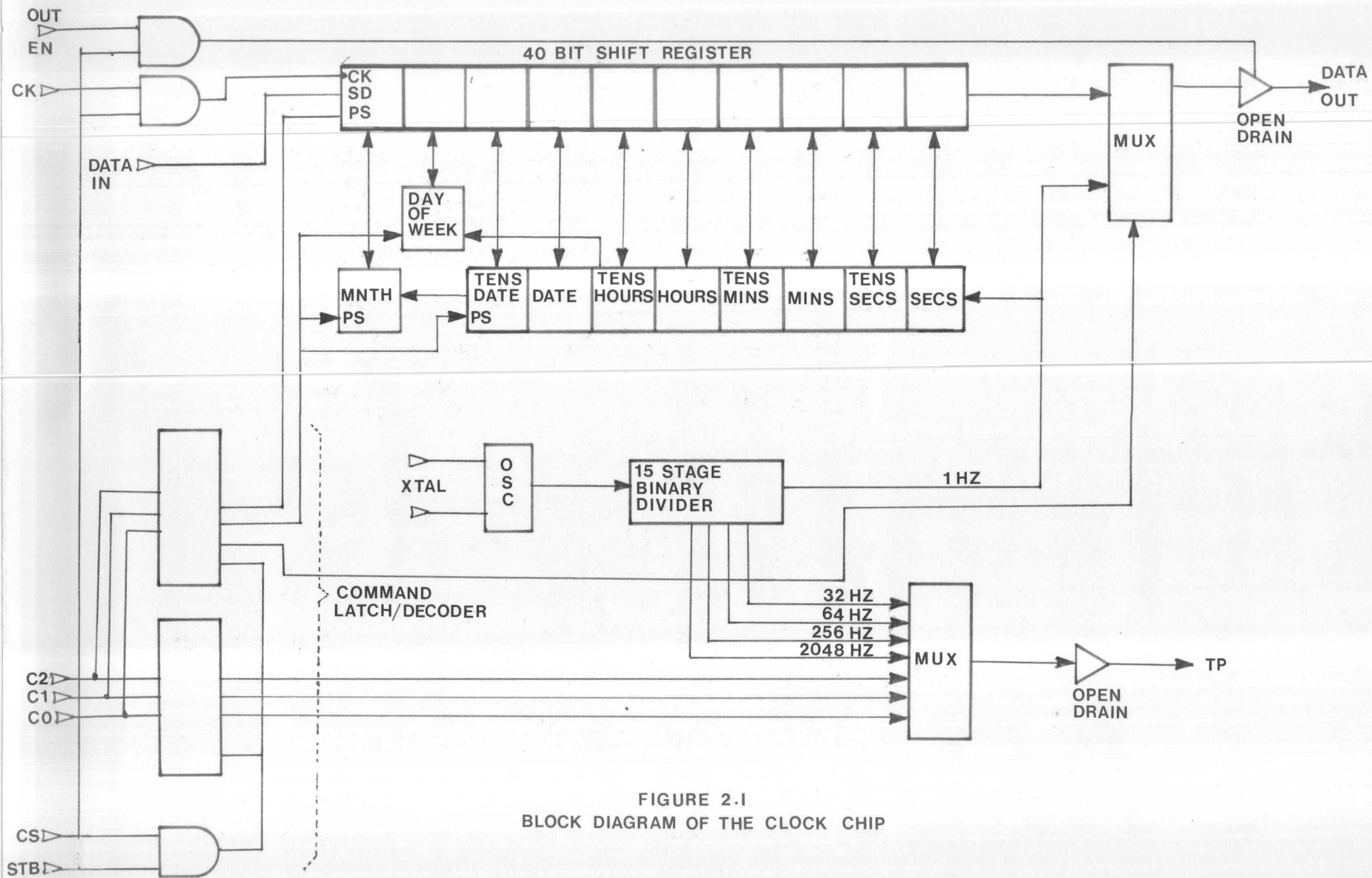


FIGURE 2.1
BLOCK DIAGRAM OF THE CLOCK CHIP

CHAPTER 3 PROGRAMMING INFORMATION

Introduction

Programming the QBX-PCC hinges on understanding the operation of the 8255A. It is recommended that the user has read the programming procedures of this device before reading this chapter.

Initialisation

Every time that the power is applied to the system the QBX-PCC must be initialised. This takes the form of programming the 8255A and then setting up to outputs to required levels.

Before any levels can be set, the 8255A must be configured for operation by writing a modeword to port location X3 or X7 hex, where X is determined by the host board. Port B must be set to Mode 0, output, and port C lower must be set to input. The remaining bits are left for the user to configure to his own requirements.

Mode Word Bit	Level	Options
D7	1	No option
D6	0/1	\User option port A mode
D5	0/1	
D4	0/1	User option port A input/output
D3	0/1	User option port C Upper
D2	0	Port B mode 0
D1	0	Port B output
D0	1	Port C lower input

Table 3.1
8255A modeword

In summary the mode word should be 1xxxx001 binary where x is left to the user.

After this port B should be set to 0 by writing 00 hex to port location X1 or X5 hex, where X is determined by the host board.

Clock Interface

Figure 2.1 is a block diagram of the internal structure of the 1990. The device is split into two sections. The first is the clock/calendar functions whilst the second provides a periodic output on TP. The action performed by the device depends on the command strobed in (a low to high transition on STB) on the command lines C0-C2. When C2=0 the command pertains to the clock/calendar and when C2=1 the command pertains to the periodic output. Each section holds its command irrespective of the function of the other.

Strobing in the Command

The different commands are made up by different combinations of C0-C2. Table 3.2 and a following section describes these commands. For the moment let us study how to strobe these commands into the device. Figure 3.1 shows the timing diagram. A sample 8085 programme is shown to achieve the required effect. In all the following examples it is assumed that the SBX board occupies the locations C0 hex to CF hex.

```

IN      0C1H          ;READING THE CONTENTS OF PORT B
ANI     11000111B     ;CLEARING PREVIOUS COMMAND
ORI     00101000B     ;FOR EXAMPLE C2=1, C1=0, C1=1
OUT     0C1H          ;SET ON OUTPUT
NOP
NOP      ;2 uS WAIT
ORI     04H           ;SETTING STB HIGH
OUT     0C1H
NOP      ;2 uS WAIT
NOP
ANI     NOT 04H        ;CLEARING STB
OUT     0C1H
.
.
.

```

A sample programme is shown in the appendix which allows for a generalised subroutine to set the command.

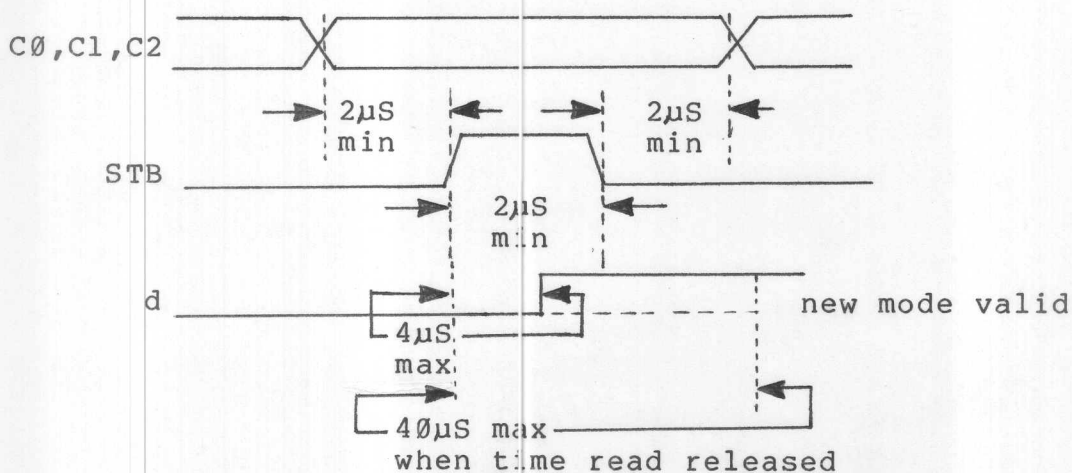


Figure 3.1
Command Timing

Flowchart 3 in the appendix shows how the command mode may be set up.

Using the Shift Register

All data communicated with the clock/calendar registers is via a 40 bit shift register. When not in use this register may be used to store critical information or even the years. It must be remembered that when reading the time the contents of this register are altered. If the register is used for this purpose care must be exercised in the case of reading and storing in the case of power fail. The dropping of Vcc below 4.5V will inhibit the register with an unknown value in it, which would prove meaningless when power is restored.

To read the clock/calendar an instruction is given to transfer the clock registers into the shift register. After a maximum of 40uS this is done. The advantage is that the data is valid without having to worry that errors had occurred during the time update, which occurs with other manufacturer's clock calendar chips.

Command SetGroup 0 Clock/Calendar

Register Hold: C0=0, C1=0, C2=0

The data in the shift register is held and shifting of the data is impossible. A square wave of 1Hz frequency appears at the data output pin. This may be used for interrupt purposes. Register hold is the normal rest condition.

Register Shift: C0=1, C1=0, C2=0

The data in the shift register is shifted out via the data out pin on the leading positive edge of the CK input. Data present on the data input is shifted onto the most significant bit simultaneously. The least significant bit corresponds to the data out pin. Flowcharts 4 and 5 demonstrate how data is clocked in and out. A sample programme follows:

```

                                ;PC0 HAS LSB VALUE
                                ;READ PORT C, USE BIT 0 VALUE
IN      0C2H                    ;TO SET CARRY
RRC
MOV     A,B                     ;B USED TO RECORD INCOMING INFO.
RAR
MOV     B,A                     ;BIT ONTO REGISTER B

;NOW TO FETCH OUTGOING DATA-IT IS NOT NECESSARY TO DO THIS
;SIMULTANEOUSLY. THIS IS JUST BEING DONE TO SHOW HOW TO SAVE TIME
;DATA TO BE STORED IS ON REGISTER C
MOV     A,C
RLC
MOV     C,A                     ;SINGLING OUT BIT
ANI     02H                     ;SAVE FOR NEXT TIME
MOV     E,A                     ;TEMPORARY SAVE
IN      0C1H                     ;CURRENT PORT B
ANI     NOT 02H                 ;CLEAR BIT
ORA     E                       ;REFLECT DATA BIT

```

```

OUT  0C1H          ;ON OUTPUT
NOP                    ;2μS DELAY
ORI   01H          ;SET CK HIGH
OUT  0C1H
NOP                    ;2μS WAIT
ANI   NOT 01H      ;CLEAR CK
OUT  0C1H
.
.
.

```

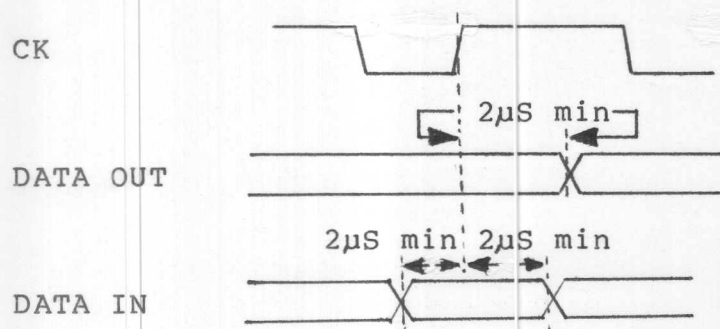


Figure 3.2
CK Timing

Time Set: C0=0, C1=1, C2=0

The data in the 40 bit shift register is preset onto the timing registers. The prescaler to all intents and purposes is reset to 0 and the clock continues from this time. The time start is the low to high transition of the STB signal. Shifting of data is impossible. Data out is the LSB of the shift register. Flowchart 1 shows how time may be set.

Time Read: C0=1, C1=1, C2=0

The value of the clock/calendar counters are transferred into the 40 bit shift register. Shifting of the data is impossible and data out is the LSB (LSB=0.5Hz). Flowchart 2 demonstrates how the time may be read.

Group 1 Programmable Frequency Output

Except for command C0=C1=C2=1 all these commands in this section alter the frequency at the TP open drain output. The waveform has a 50% duty cycle. These may be used for interrupts and for calibration.

64 Hz: C0=0, C1=0, C2=1

256 Hz: C0=1, C1=0, C2=1

2048 Hz: C0=0, C1=1, C2=1

Test: C0=1, C1=1, C2=1

Do NOT use this mode at all as unpredictable results may occur.

Using the Clock

A sample programme is shown in the appendix. Figure 3.3 overleaf demonstrates reading and writing time information to and from the 1990.

The QBX-PCC does recognise February 29 when set, but does not change to this automatically. This may be done through software. For this adjustment the year must be known. This may be saved in the 40 bit shift register during power down or on a permanent basis shifting it out prior to reading the time. The user is reminded of the earlier caution in the section "Using the Shift Register".

The allocation of bits on read or write is as follows in table 3.2

Bits	Function
0-3	Seconds
4-7	10s Seconds
8-11	Minutes
12-15	10s Minutes
16-19	Hours
20-23	10s Hours
24-27	Date
28-31	10s Date
32-35	Day of Week
36-40	Month

Table 3.2
Allocation of bits in Shift Register

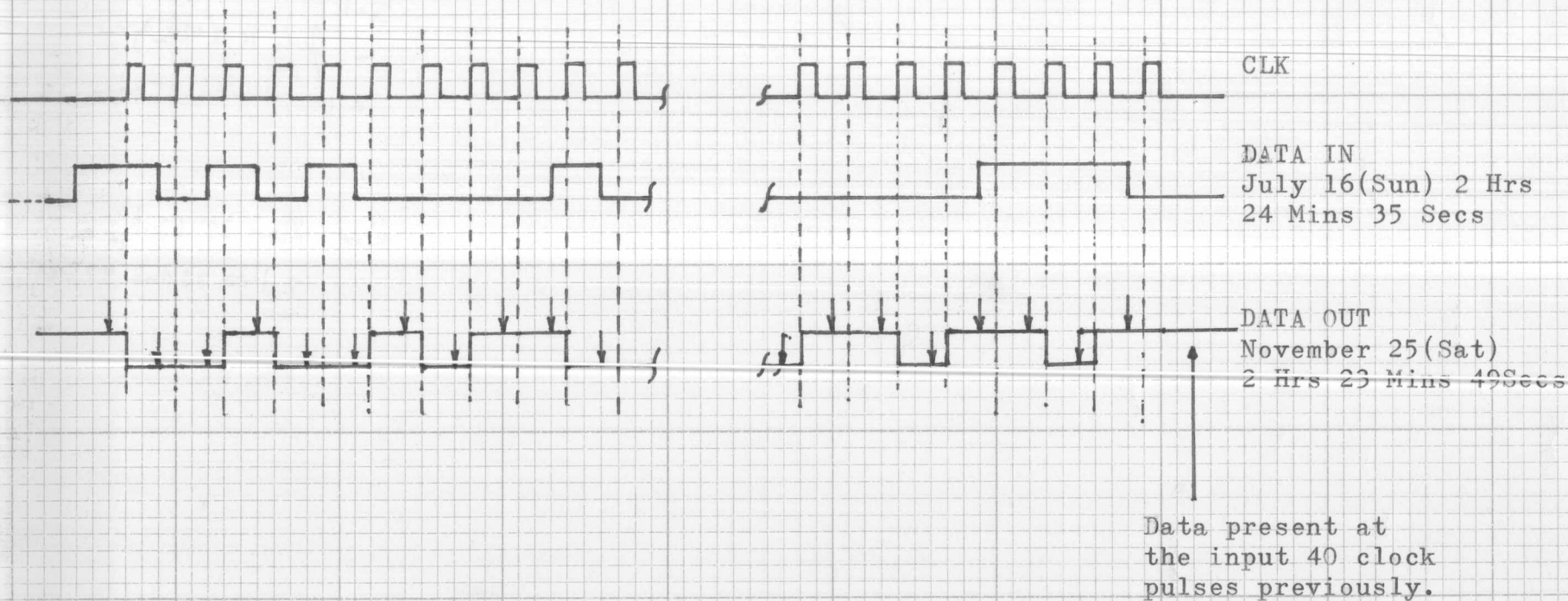
All information is in BCD with the exception of the months which go from 01H to 0CH. Days go from 0H to 6H.

Summary of Commands

C0	C1	C2	Data out	T.P.	Title
0	0	0	1 Hz	Unchanged	Hold
1	0	0	LSB	Unchanged	Shift
0	1	0	LSB	Unchanged	Time Set
1	1	0	LSB	Unchanged	Time Read
0	0	1	Unchanged	64 Hz	
1	0	1	Unchanged	256 Hz	
0	1	1	Unchanged	2048 Hz	
1	1	1	DO NOT USE		Test

Table 3.3
Summary of 1990 Clock/Calendar Functions

Group 0 and group 1 commands hold their functions independently.



SHIFTING DATA IN AND OUT OF THE CLOCK CHIP

Note: All data is shifted in or out on the leading low to high transition of the CLK.

FIG 3.3

CHAPTER 4 PREPARATION FOR USE

Introduction

This chapter provides information on the installation of the QBX-PCC on a host SBC board.

Unpacking

The QBX-PCC is shipped in a padded packet together with 1 plastic spacer and 2 plastic screws.

On receipt of the package inspect immediately for signs of damage, water or any other signs of mishandling. If there are any of these signs contact your carrier or his agent, or the local R & D Electronics representative. If you do open the package, please retain the packaging.

Mounting

The QBX-PCC will mount on any SBC computer that allows an iSBX board. Affix the spacer with one of the screws to the host board. Mount the spacer in the hole corresponding to the hole on the QBX board next to R5.

The QBX-PCC should now be mounted on the mating connector and affixed to the host board with the remaining screw.

When a QBX card is mounted on a host card, the resulting structure occupies an additional card slot above the SBC card. Bear this in mind when you allocate slots in a cardframe.

Battery

If the on board battery is to be used, then the battery connection wire should be soldered to the positive terminal of the battery.

Calibration

The crystal frequency has not been adjusted at the factory. To calibrate it is possible to measure the frequency at IC2/13. The capacitance of the probe may affect the frequency of oscillation so through software or in-circuit emulation set up mode 6 and monitor TP (IC2/10) for 2048 Hz.

CHAPTER 5 SERVICE

Introduction

This chapter provides a parts list and a schematic diagram of the QBX-PCC.

Parts List

Semiconductors:

IC1	Programmable Peripheral Interface	8255A-5
IC2	NEC CMOS serial I/O clock/calendar	uPD1990AC
IC3	Quad comparator	LM339
IC4/5	Not supplied	

D1	General purpose diode	1N4001
----	-----------------------	--------

Capacitors:

C1	ceramic	22 pF
C2,C3	ceramic	0.01uF
VC1	trimmer	4-40pF

Resistors:

RA1	resistor array	898-3-R100K
R1	1/4W 2%	120 Kohm
R2	1/4W 2%	39 Kohm
R3	1/4W 5%	82 ohm
R4,5	1/4W 2%	150 Kohm
R6,10	1/4W 2%	100 Kohm
R7,9	1/4W 5%	10 Kohm
R8	1/4W 5%	4.7 Kohm

Crystal:

X1	ceramic crystal	32768 Hz
----	-----------------	----------

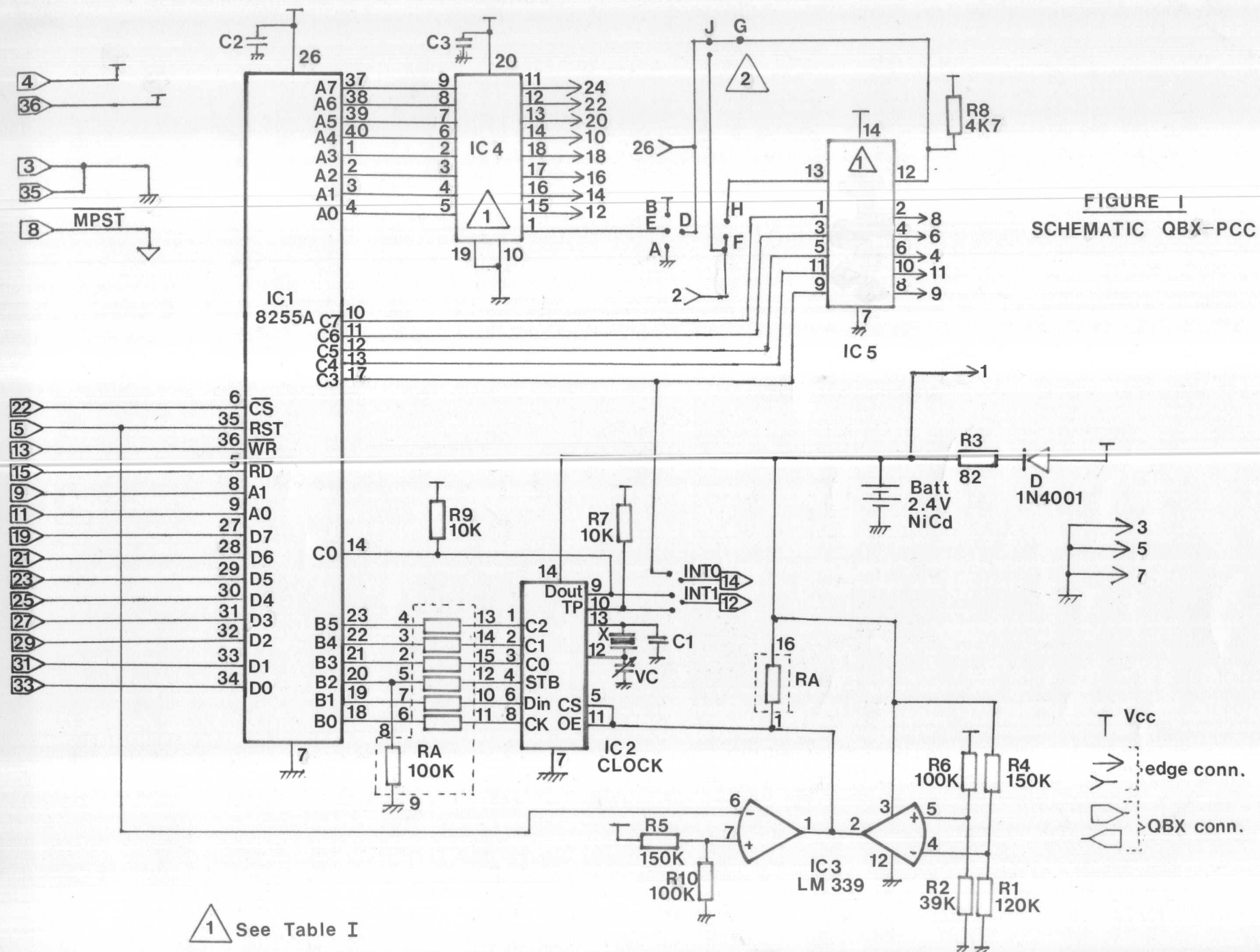
Battery:

Eveready 2.4V 0.15AH NiCd	NCB 15Z2A
---------------------------	-----------

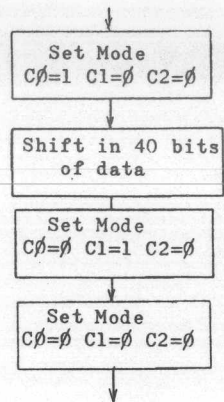
Connector:

Viking 36 way SBX	LMP01KH18A01
-------------------	--------------

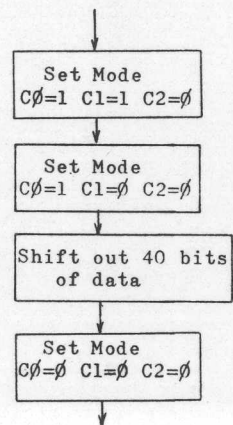
Unused parts:



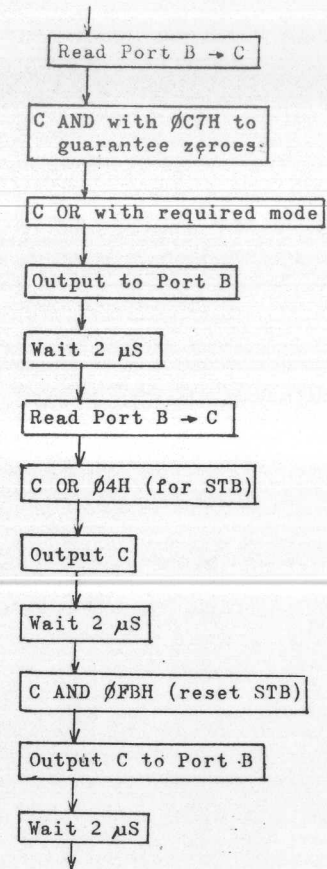
APPENDIX A
FLOW CHARTS



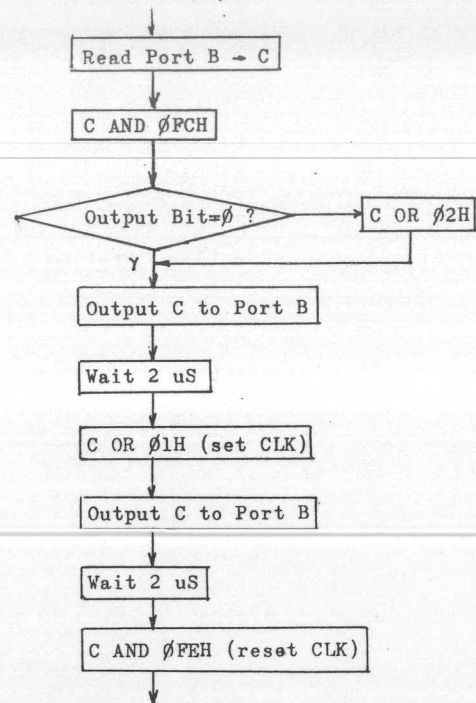
Flow Chart 1
Time Set.



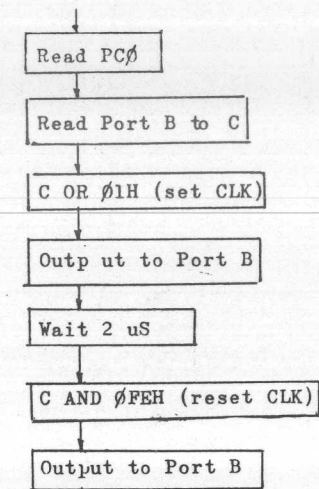
Flow Chart 2
Time Read



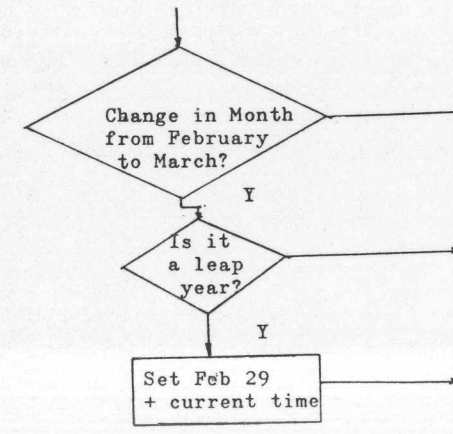
Flow Chart 3
Set up Mode.



Flow Chart 4
Clocking a single bit of
data into the Clock/Calendar



Flow Chart 5
Reading a single bit of data
from the Clock/Calendar.



Flow Chart 6
Leap Year adjustment for Feb 29.

**APPENDIX B
SAMPLE PROGRAMME**

LOC	OBJ	LINE	SOURCE STATEMENT
		12	DSEG
0000		13	SECOND: DS 1
0001		14	MINUTE: DS 1
0002		15	HOUR: DS 1
0003		16	DATE: DS 1
0004		17	DAY: DS 1
0005		18	MONTH: DS 1
0006		19	YEAR: DS 1
		20	;
		21	*****
00E0		22	PORTA EQU 0E0H
00E1		23	PORTB EQU 0E1H
00E2		24	PORTC EQU 0E2H
00E3		25	CNTL EQU 0E3H
0089		26	MDWD EQU 89H
0001		27	TWOMIC EQU 1 ;1uS DELAY
0014		28	FTYMIC EQU 20 ;40uS DELAY
		29	;
		30	*****
		31	CSEG
0000 C317A1 C		32	JMP TEST
		33	;
		34	*****
		35	CLKINT:
		36	;CLOCK INITIALISE
		37	;SET 8255 AS FOLLOWS
		38	;PORT A-OPTIONAL SET AS MODE 0 OUTPUT
		39	;PORT C UPPER-OPTIONAL INPUT
		40	;PORT B MODE 0 OUTPUT
		41	;PORT C LOWER INPUT
		42	;THE IO ADDRESS MAP IS FOR 8 ADDRESSES.
		43	;THE UPPER 4 WILL OVERWRITE THE LOWER 4
		44	;I.E. ADDRESS F0H IS IDENTICAL TO F4H
		45	;PORT A=F0
		46	;PORT B=F1
		47	;PORT C=F2
		48	;CONTROL=F3
		49	;
0003 3E89		50	MVI A,MDWD
0005 D3E3		51	OUT CNTL
		52	;
		53	;SET PORT B TO ALL ZEROES
0007 3E00		54	MVI A,0
0009 D3E1		55	OUT PORTB
		56	;
		57	;NOW TO LATCH MODE 0 ON CLOCK
000B 0E00		58	MVI C,0
000D CD2600 C		59	CALL STMODE
0010 C9		60	RET
		61	;
		62	*****
		63	;
		64	CLKPIN:

LOC	OBJ	LINE	SOURCE STATEMENT
		65	;THIS WILL SET AND RESET THE CLOCK PIN ON THE CLOCK CHIP
0011 DBE1		66	IN PORTB
		67	;READING IN TO PRESERVE THE STATUS OF THE OTHER OUTPUTS.
0013 F601		68	ORI 01H
0015 D3E1		69	OUT PORTB
0017 CD4600 C		70	CALL WAIT
		71	;IN LINE PARAMETER
001A 01		72	DB TWOMIC
		73	;DELAY FOR SETTLING TIME
001B DBE1		74	IN PORTB
001D E6FE		75	ANI 0FEH
001F D3E1		76	OUT PORTB
0021 CD4600 C		77	CALL WAIT
0024 01		78	DB TWOMIC
0025 C9		79	RET
		80	;
		81	*****
		82	;
		83	STMODE:
		84	;THIS ROUTINE SETS THE MODE ON THE CLOCK ACCORDING
		85	;TO THE PARAMETER FED THROUGH ON THE C REGISTER
		86	;
		87	;SAVING THE CURRENT VALUES OF PSW AND BC
0026 C5		88	PUSH B
0027 F5		89	PUSH PSW
		90	;
		91	;CONSTRUCTING OUTPUTS FOR C0 TO C2
		92	;ON PORT B WITHOUT AFFECTING OTHER OUTPUTS
0028 DBE1		93	IN PORTB
002A E6C7		94	ANI 11000111B
002C B1		95	ORA C
002D D3E1		96	OUT PORTB
		97	;
		98	;2uS DELAY MINIMUM
002F CD4600 C		99	CALL WAIT
0032 01		100	DB TWOMIC
		101	;
		102	;NOW TO STROBE THIS IN
		103	;
0033 DBE1		104	IN PORTB
0035 F604		105	ORI 04H
0037 D3E1		106	OUT PORTB
0039 CD4600 C		107	CALL WAIT
003C 01		108	DB TWOMIC
		109	;
		110	;RESETTING STROBE LINE
003D DBE1		111	IN PORTB
003F E6FB		112	ANI 11111011B
0041 D3E1		113	OUT PORTB
		114	;
0043 F1		115	POP PSW
0044 C1		116	POP B
0045 C9		117	RET

LOC	OBJ	LINE	SOURCE STATEMENT
		118 ;	
		119 ;*****:	
		120 WAIT:	
		121 ;TIME DELAY SET UP BY IN-LINE PARAMETER	
		122 ;	
0046	E1	123	POP H ;RETURN ADDRESS ON HL
0047	5E	124	MOV E,M ;FETCH PARAMETER TO E
0048	23	125	INX H ;NEXT ADDRESS
0049	E5	126	PUSH H ;RESTORE NEW RETURN ADDRESS
		127 ;	
		128 WT1:	
004A	00	129	NOP
004B	00	130	NOP
004C	00	131	NOP
004D	1D	132	DCR E
004E	C24A00	133	JNZ WT1
		134 ;	
0051	C9	135	RET
		136 ;	
		137 ;*****	
		138 ;	
		139 WRT4BT:	
		140 ;WRITE 4 BITS TO THE OUTPUT TO BE SHIFTED ONTO DATA IN	
		141 ;THE 4 BITS ARE ON THE C REGISTER	
		142 ;	
0052	F5	143	PUSH PSW
0053	C5	144	PUSH B
0054	0604	145	MVI B,4
		146 WRT4B1:	
		147 ;ROTATING C RIGHT	
		148 ;AND SETTING OR CLEARING THE RELEVANT BIT	
0056	DBE1	149	IN PORTB
0058	E6FD	150	ANI 11111101B
005A	F5	151	PUSH PSW
005B	79	152	MOV A,C
005C	0F	153	RRC
005D	4F	154	MOV C,A
005E	DA6500	155	JC WRT4B2
		156 ;	
0061	F1	157	POP PSW
0062	C36800	158	JMP WRT4B3
		159 WRT4B2:	
0065	F1	160	POP PSW
0066	F602	161	ORI 02H
		162 WRT4B3:	
0068	D3E1	163	OUT PORTB
006A	CD1100	164	CALL CLKPIN
006D	05	165	DCR B
006E	C25600	166	JNZ WRT4B1
		167 ;	
0071	C1	168	POP B
0072	F1	169	POP PSW
0073	C9	170	RET

LOC	OBJ	LINE	SOURCE STATEMENT
		171 ;	
		172 ;*****	
		173 ;	
		174 RD4BIT:	
		175 ;READS 4 BITS AND RETURNS WITH 4 BITS ON ACCUMULATOR	
		176 ;	
0074	C5	177	PUSH B
		178 ;	
0075	0604	179	MVI B,4
0077	0E00	180	MVI C,0
		181 RD4BI1:	
0079	DBE2	182	IN PORTC
007B	0F	183	RRC
		184 ;SET CARRY BIT WITH INCOMING DATA	
		185 ;AND MOVE ONTO C	
007C	79	186	MOV A,C
007D	1F	187	RAR
007E	4F	188	MOV C,A
		189 ;	
		190 ;CLOCK NEXT BIT OUT	
007F	CD1100	191	CALL CLKPIN
0082	05	192	DCR B
0083	C27900	193	JNZ RD4BI1
		194 ;	
		195 ;ROTATING TO GET IT TO LEAST SIGNIFICANT NIBBLE	
0086	79	196	MOV A,C
0087	0F	197	RRC
0088	0F	198	RRC
0089	0F	199	RRC
008A	0F	200	RRC
008B	E60F	201	ANI 0FH
		202 ;	
008D	C1	203	POP B
008E	C9	204	RET
		205 ;	
		206 ;*****	
		207 ;	
		208 WRT8BT:	
		209 ;WRITE 8 BITS FED IN ON C	
		210 ;	
008F	C5	211	PUSH B
		212 ;	
0090	79	213	MOV A,C
0091	E60F	214	ANI 0FH
0093	4F	215	MOV C,A
0094	CD5200	216	CALL WRT4BT
		217 ;LEAST SIGNIFICANT NIBBLE FIRST	
		218 ;	
0097	C1	219	POP B
0098	C5	220	PUSH B
		221 ;	
0099	79	222	MOV A,C
009A	0F	223	RRC

LOC	OBJ	LINE	SOURCE STATEMENT
009B	0F	224	RRC
009C	0F	225	RRC
009D	0F	226	RRC
009E	E60F	227	ANI 0FH
00A0	4F	228	MOV C,A
00A1	CD5200	229	CALL WRT4BT
00A4	C1	230	AND THEN MOST SIGNIFICANT NIBBLE
00A5	C9	231	POP B
		232	RET
		233	;
		234	*****
		235	RD8BIT:
		236	READS 8 BITS IN AND RETURNS WITH RESULT ON THE ACCUMULATOR
00A6	C5	237	PUSH B
		238	;
00A7	CD7400	239	CALL RD4BIT
00AA	F5	240	PUSH PSW
00AB	CD7400	241	CALL RD4BIT
		242	;
00AE	07	243	RLC
00AF	07	244	RLC
00B0	07	245	RLC
00B1	07	246	RLC
00B2	E6F0	247	ANI 0F0H
00B4	4F	248	MOV C,A
00B5	F1	249	POP PSW
00B6	B1	250	ORA C
00B7	C1	251	POP B
		252	;
00B8	C9	253	RET
		254	;
		255	*****
		256	;
		257	RDTIME:
		258	READS TIME AND STORES THE RESULT IN THE RELEVANT LOCATIONS
		259	WE ASSUME THAT THE LOCATIONS ARE CONTIGUOUS STARTING
		260	WITH SECONDS AS DEFINED ABOVE
		261	;
		262	WE FIRST SET MODE
00B9	0E18	263	MVI C,00011000B
00BB	CD2600	264	CALL STMODE
00BE	0E08	265	MVI C,00001000B
00C0	CD2600	266	CALL STMODE
		267	;
		268	WAITING INSTRUCTION TIME td 40us
00C3	CD4600	269	CALL WAIT
00C6	14	270	DB FTYMIC
		271	;
00C7	210000	272	LXI H,SECOND
00CA	0604	273	MVI B,4
		274	;

LOC	OBJ	LINE	SOURCE STATEMENT
		275	RDTIM1:
00CC	E5	276	PUSH H
00CD	CDA600	277	CALL RD8BIT
00D0	E1	278	POP H
00D1	77	279	MOV M,A
		280	;
00D2	23	281	INX H
00D3	05	282	DCR B
00D4	C2CC00	283	JNZ RDTIM1
		284	;
		285	THIS HAS READ IN UP TO AND INCLUDING DATE, LEAVING DAY AND MONTH
		286	;
00D7	0602	287	MVI B,2
		288	RDTIM2:
00D9	E5	289	PUSH H
00DA	CD7400	290	CALL RD4BIT
00DD	E1	291	POP H
00DE	77	292	MOV M,A
00DF	23	293	INX H
00E0	05	294	DCR B
00E1	C2D900	295	JNZ RDTIM2
		296	;
		297	RESETTING MODE
00E4	0E00	298	MVI C,00000000B
00E6	CD2600	299	CALL STMODE
00E9	C9	300	RET
		301	;
		302	*****
		303	;
		304	SETTIM:
		305	SET TIME BUT DOES NOT CHECK FOR ILLEGAL FORMAT OR
		306	INVALID TIMES OR DATES
		307	;
		308	SETTING MODE TO SHIFT
00EA	0E08	309	MVI C,00001000B
00EC	CD2600	310	CALL STMODE
		311	;
00EF	210000	312	LXI H,SECOND
00F2	0604	313	MVI B,4
		314	;
		315	SETTI1:
00F4	E5	316	PUSH H
00F5	4E	317	MOV C,M
00F6	CD8F00	318	CALL WRT8BT
00F9	E1	319	POP H
00FA	23	320	INX H
00FB	05	321	DCR B
00FC	C2F400	322	JNZ SETTI1
		323	;
		324	NOW FOR DAY AND MONTH
00FF	0602	325	MVI B,2
		326	SETTI2:

LOC	OBJ	LINE	SOURCE STATEMENT
0143	210100	D 378	LXI H,SECOND+1
0146	0E05	379	MVI C,5
0148	78	380	MOV A,B
		381	TEST5:
0149	BE	382	CMP M
014A	C26801	C 383	JNZ TEST6
		384	;
014D	23	385	INX H
014E	0D	386	DCR C
014F	C24901	C 387	JNZ TEST5
		388	;AT THIS POINT EQUALITY
		389	;SO WE CLOCK THE LED
0152	D3D6	390	OUT 0D6H
0154	00	391	NOP
0155	00	392	NOP
0156	00	393	NOP
0157	CD4600	C 394	CALL WAIT
015A	FF	395	DB 0FFH
015B	C1	396	POP B
015C	DBE0	397	IN PORTA
015E	07	398	RLC
015F	D3E0	399	OUT PORTA
0161	05	400	DCR B
0162	C22301	C 401	JNZ TEST2A
0165	C32101	C 402	JMP TEST1
		403	TEST6:
0168	C36801	C 404	JMP TEST6
		405	;
		406	END

PUBLIC SYMBOLS

EXTERNAL SYMBOLS

USER SYMBOLS

CLKINT C 0003	CLKPIN C 0011	CNTL A 00E3	DATE D 0003
DAY D 0004	FTYMIC A 0014	HOUR D 0002	MDWD A 0089
MINUTE D 0001	MONTH D 0005	PORTA A 00E0	PORTB A 00E1
PORTC A 00E2	RD4BIT C 0079	RD4BIT C 0074	RD8BIT C 00A6
RDTIM1 C 00CC	RDTIM2 C 00D9	RDTIME C 00B9	SECOND D 0000
SETTI1 C 00F4	SETTI2 C 0101	SETTIM C 00EA	STMODE C 0026
TEST C 0117	TEST1 C 0121	TEST2 C 0128	TEST2A C 0123
TEST3 C 012E	TEST4 C 0137	TEST5 C 0149	TEST6 C 0168
TWDMIC A 0001	WAIT C 0046	WRT4B1 C 0056	WRT4B2 C 0065
WRT4B3 C 0068	WRT4BT C 0052	WRT8BT C 008F	WT1 C 004A
YEAR D 0006			

ASSEMBLY COMPLETE, NO ERRORS